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*Karen Cinq-Mars 3/15/04*  
(Signature & date)

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Re application of \_\_\_\_\_ : March 15, 2004  
Rama Divakaruni, et al. \_\_\_\_\_ : Group Art Unit: to be assigned  
Serial No. 10/708,530 \_\_\_\_\_ : Examiner: to be assigned  
Filed: 3/10/04 \_\_\_\_\_ : International Business Machines Corporation  
2070 Route 52  
Hopewell Junction, NY 12533

**TITLE:** METHOD FOR MANUFACTURING TUNGSTEN/POLYSILICON WORD LINE STRUCTURE  
IN VERTICAL DRAM AND DEVICE MANUFACTURED THEREBY

**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Pursuant to the duty of disclosure set forth in 37 C.F.R. 1.56, and further pursuant to the provisions of 37 C.F.R. 1.97 and 1.98, applicants hereby respectfully submit copies of the non-US patents and publications as listed on Form PTO-1449, attached hereto.

In citing these documents, no representation is made nor intended as to the pertinency or non-pertinency of the art, that better art than that listed is not available, or that other art is not applicable.

No fee is believed to be due for this submission. If any fees are required, however, the Commissioner is hereby authorized to charge such fees to Deposit Account No. 09-0458.

Respectfully submitted,  
Rama Divakaruni, et al.

By \_\_\_\_\_

*H. Daniel Schurmann*  
H. Daniel Schurmann  
Registration No. 35,791  
Telephone No. 845-894-2481

# INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)

FIS920030421US1

Application Number

10/708,530

Applicant(s)

Rama Divakaruni, et al.

Filing Date

March 10, 2004

Group Art Unit

Not Yet Assigned

## U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

## FOREIGN PATENT DOCUMENTS

	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
							YES	NO

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

		Divakaruni et al. "Gate Prespacers for High Density DRAMS" International Symposium on VLSI Technology Systems and Applications, Taipei, Taiwan (8-10 June 1999)
		Akatsu et al., "A Highly Manufacturable 110nm DRAM Technology with 8F2 Vertical Transistor Cell for 1Gb and Beyond"; Symposium on VLSI Technology; pp 52-53 (2002)

EXAMINER	DATE CONSIDERED
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EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.